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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,394	12/28/2001	Seong-jae Lee	2013p006	8538

8791 7590 10/17/2003

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 10/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	10/033,394	LEE ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- Th MAILING DATE of this communication appears on th cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/15/2003 has been entered. A new rejection is made as set forth in this Office Action. Claims (1-5 and 7-20) are pending in the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 and 7-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byun et al. (U.S. Patent 5,599,734) in view of Kroner et al. (IEEE 2000).

Byun teaches a method of fabricating an integrated circuit comprising (col. 3, line 29 to col. 4, line 17 and FIGS. 2(a-c)):

forming a diffusion barrier layer pattern (FIGS. 2a-c: 22, 23) on a semiconductor substrate (FIGS. 2a-c: 21) (col. 3, lines 29-32);

forming a SOG layer (FIGS. 2a-c: 24) containing impurities, including either one of a p-type impurity and an n-type impurity on the entire surface of the semiconductor

substrate wherein the SOG layer is formed by spin-coating and densifying a liquid silicate glass or CVD including P and B doping elements (col. 3, lines 33-57 and FIG. 2b) and wherein the ratio of the thickness of the SOG layer to the height of a gate electrode constituting the gate pattern is between 1:1.5 and 1:10; and

diffusing the impurity ions contained in the SOG layer into the semiconductor substrate by a solid phase diffusion method using rapid thermal annealing at a temperature of 800-1100 °C (col. 4, line 17) to form shallow junctions having a LDD region self-aligned underneath both sidewalls of the gate pattern and a highly doped source/drain region (FIG. 2c: 25) adjacent to the LDD region (col. 3, lines 38-40) wherein the shallow junctions having a doping depth of 50nm or less (col. 4, lines 26-28).

Byun fails to explicitly disclose additionally implanting impurity ions into portions of the SOG layer formed on the diffusion barrier layer and the semiconductor substrate by a plasma ion implantation method to increase the concentration of impurities in the SOG layer using a plasma ion implanter including a Plasma Immersion Ion Implanter (PIII) and an Ion Shower Implanter (ISI) as recited in present claims 1, 4, 11 and 15.

Kroner et al. disclose (page 476) additionally implanting impurity ions into the SOG layer by a plasma ion implantation method using a plasma ion implanter including an Ion Shower Implanter (ISI). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Byun and Kroner to enable the process of additionally implanting impurity ions into portions of the SOG layer formed on the diffusion barrier layer and the semiconductor substrate by a plasma

ion implantation of Byun to be performed and furthermore to increase the concentration of impurities in the SOG layer because it is a doping method for high dose and low energy implants (page 476, Abstract).

Byun fails to explicitly disclose the ranges for the maximum impurity implantation concentration of the SOG layer and doping concentration of the shallow junctions as recited present claims 5, 10, 16 and 20.

However, there is no evidence indicating that the ranges for the maximum impurity implantation concentration of the SOG layer and doping concentration of the shallow junctions are critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Response to Amendment

Response to Arguments

Applicant's arguments filed 09/15/2003 have been fully considered but they are not persuasive.

In response to applicant's argument that Byun fails to teach an SOG layer containing impurities, including either one of a p-type impurity and an n-type impurity,

on the entire surface of the semiconductor substrate, as requited by Claims 1 and 11, examiner respectfully disagree, Byun (U.S. Patent 5,599,734) discloses forming a SOG layer (FIG. 2b: 24) having a first conductivity type impurity (n-type impurity such as phosphorous (P)) and a second conductivity impurity (p-type impurity such as Boron (B)) of a higher concentration than that of the first conductivity impurity (col. 3, lines 33-57) over the entire surface of the semiconductor substrate (FIG. 2b: 21).

In response to applicant's argument that Byun fails to provide any teachings or suggestions with regards to the additional implanting of impurity ions into the SOG layer by a plasma ion implantation method, examiner respectfully disagree, Kroner et al. (IEEE 2000) is being used as a secondary reference in combination with Byun to disclose (page 476) additionally implanting impurity ions into the SOG layer by a plasma ion implantation method using a plasma ion implanter including an Ion Shower Implanter (ISI) to increase the concentration of impurities in the SOG layer since it is a doping method for high dose and low energy implants (page 476, Abstract). For these reasons, the rejection is considered proper

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
October 3, 2003

W. DAVID COLEMAN
PRIMARY EXAMINER